FAIRCHILD SEMICONDUCTOR®

November 2011

UniFET-II™

FDD3N50NZ

N-Channel MOSFET

500V, 2.5A, 2.5Ω

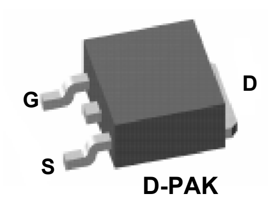
Features

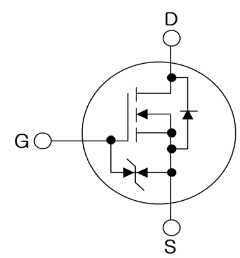
- $R_{DS(on)}$ = 2.1Ω (Typ.)@ V_{GS} = 10V, I_D = 1.25A
- Low Gate Charge (Typ. 6.2nC)
- Low C_{rss} (Typ. 2.5pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Imoroved Capability
- RoHS Compliant

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FDD3N50NZ	Units
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±25	V
I_D	Drain Current	-Continuous (T_C = 25°C)	2.5	A
		-Continuous (T_C = 100°C)	1.5	
I_{DM}	Drain Current	- Pulsed (Note 1)	10	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	114	mJ
I_{AR}	Avalanche Current	(Note 1)	2.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10	V/ns
P_D	Power Dissipation	(T_C = 25°C)	40	W
		- Derate above 25°C	0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	90	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3N50NZ	FDD3N50NZTM	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_C = 25^oC$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.5	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 400V$, $V_{GS} = 0V$, $T_C = 125^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25V$, $V_{DS} = 0V$	-	-	±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 1.25A$	-	2.1	2.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20V$, $I_D = 1.25A$ (Note 4)	-	1.9	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	210	280	pF
C_{oss}	Output Capacitance		-	30	45	pF
C_{rss}	Reverse Transfer Capacitance		-	2.5	5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400V$ $I_D = 2.5A$ $V_{GS} = 10V$ (Note 4, 5)	-	6.2	8	nC
Q_{gs}	Gate to Source Gate Charge		-	1.4	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	3.1	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 2.5A$ $V_{GS} = 10V$, $R_{GEN} = 25\Omega$ (Note 4, 5)	-	10	30	ns
t_r	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	60	ns
t_f	Turn-Off Fall Time		-	17	45	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	2.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	10	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 2.5A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 2.5A$ $dI_F/dt = 100A/\mu s$ (Note 4)	-	190	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.52	-	μC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 36.6mH, $I_{AS} = 2.5A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \leq 2.5A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test: Pulse width $\leq 300\mu s$, Dual Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

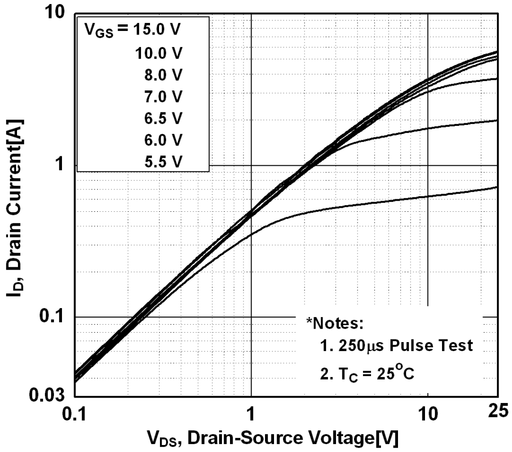


Figure 2. Transfer Characteristics

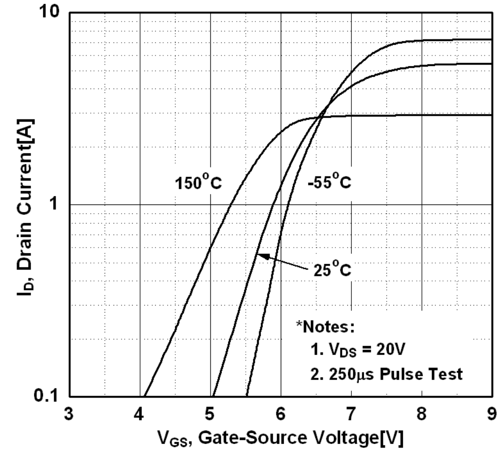


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

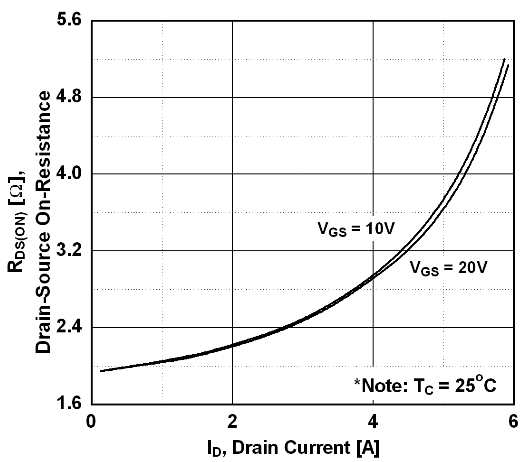


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

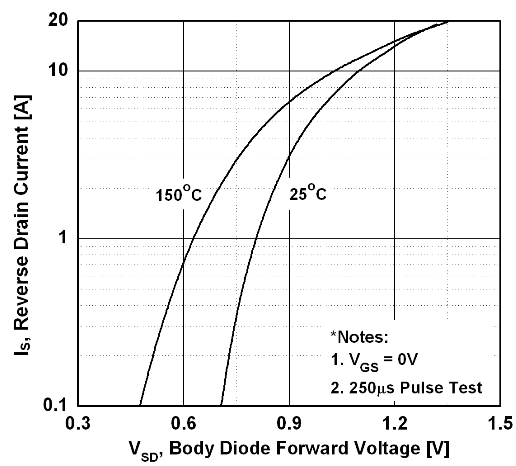


Figure 5. Capacitance Characteristics

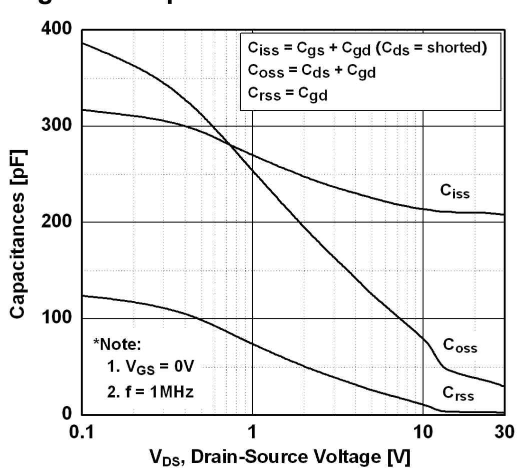
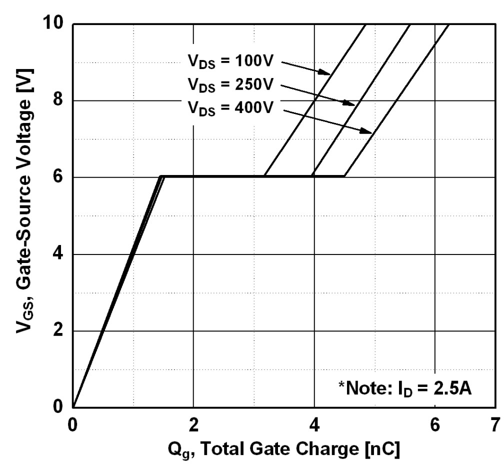


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

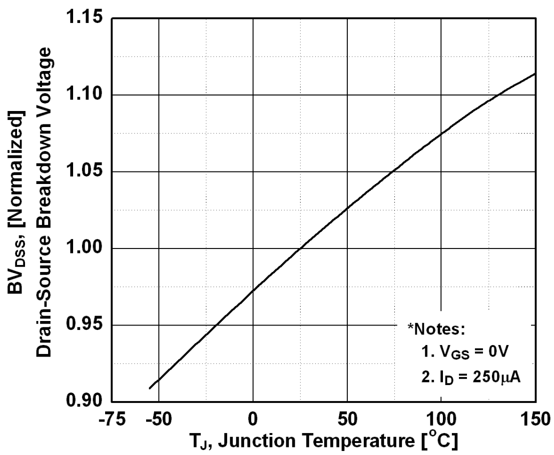


Figure 8. On-Resistance Variation vs. Temperature

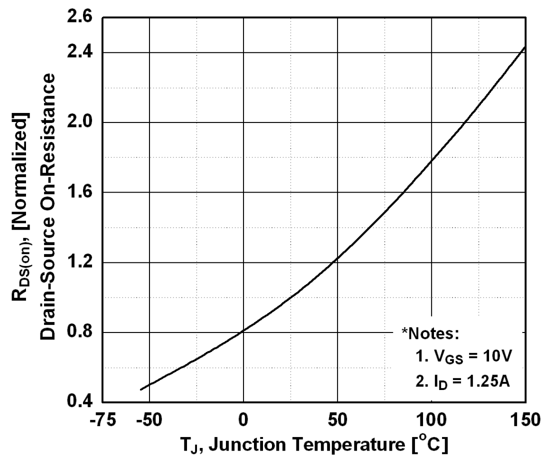


Figure 9. Maximum Safe Operating Area vs. Case Temperature

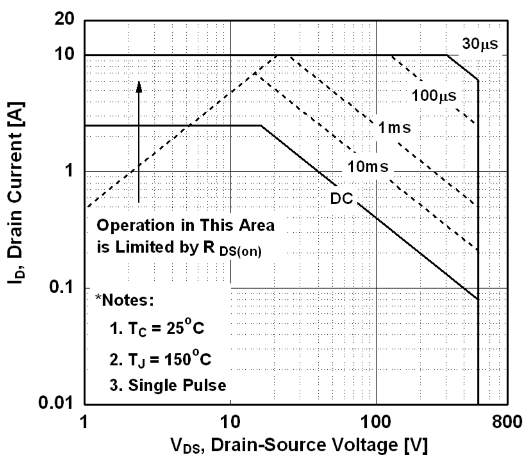


Figure 10. Maximum Drain Current

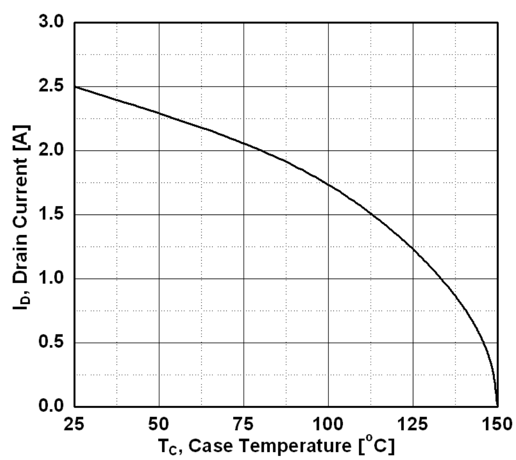
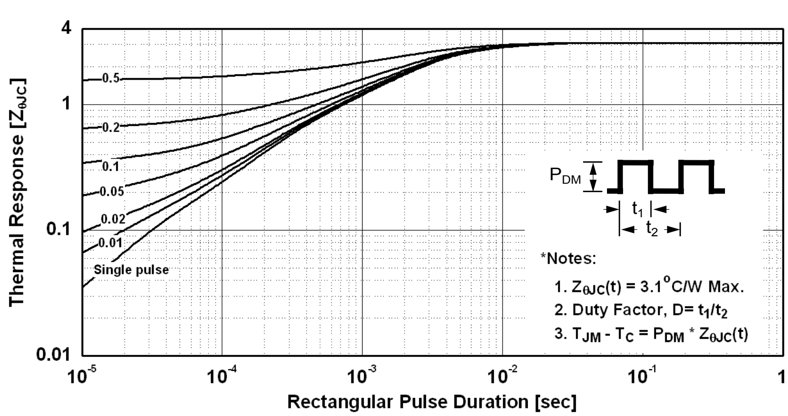
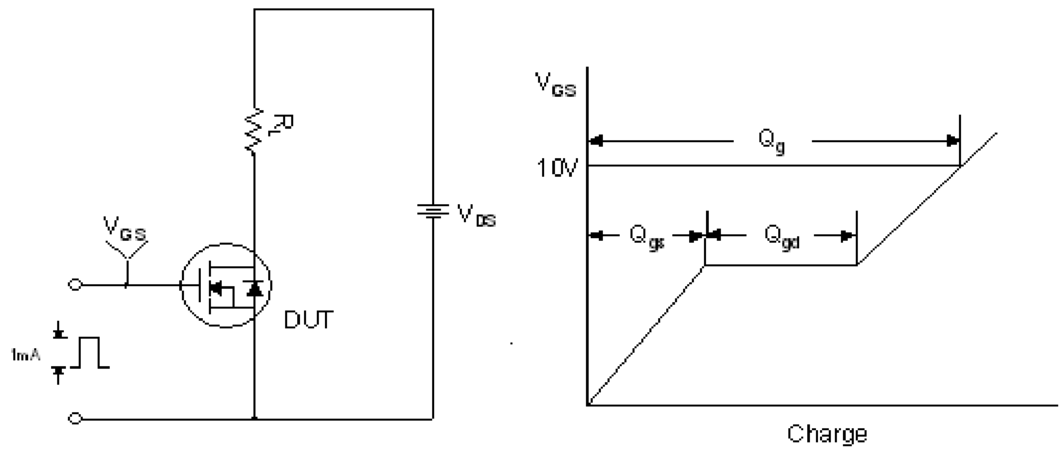


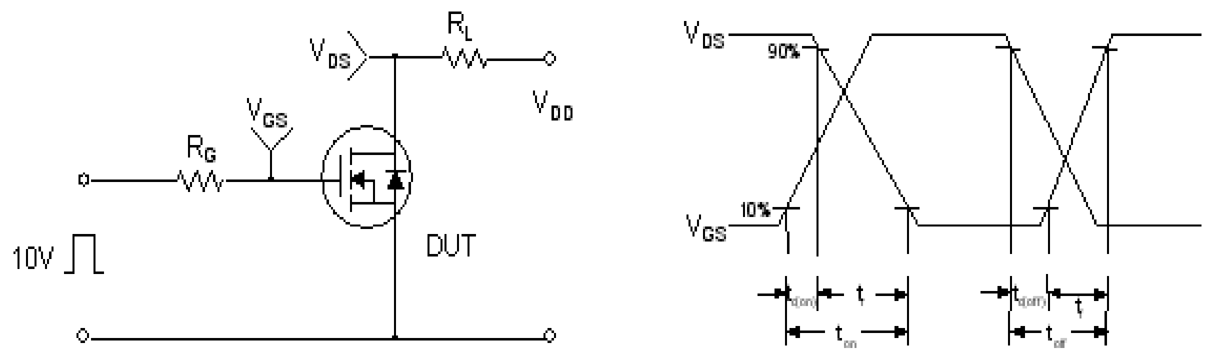
Figure 11. Transient Thermal Response Curve



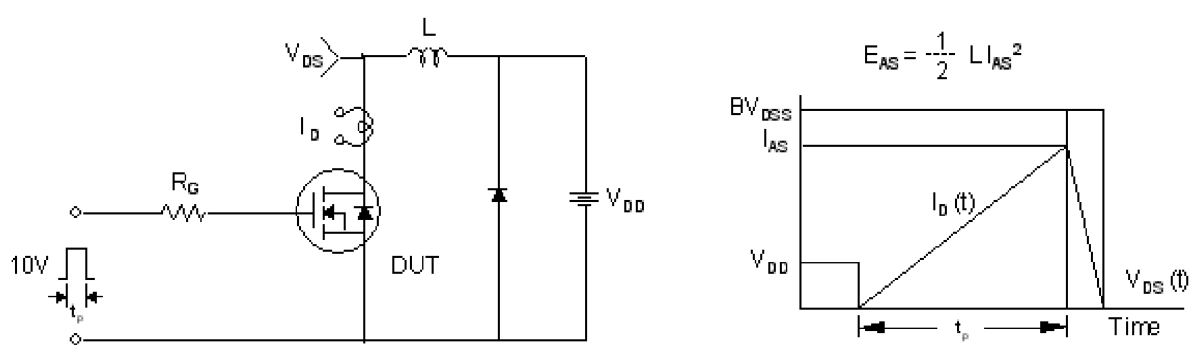
Gate Charge Test Circuit & Waveform



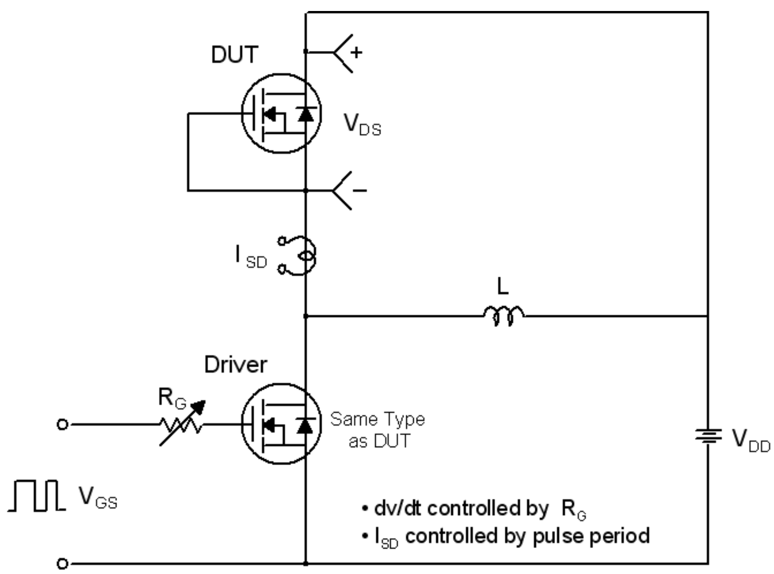
Resistive Switching Test Circuit & Waveforms

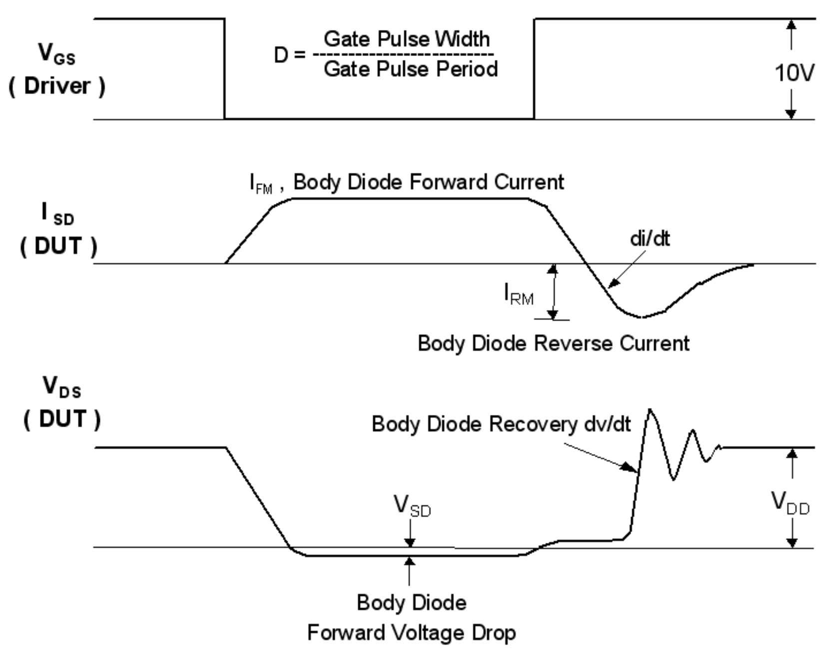


Unclamped Inductive Switching Test Circuit & Waveforms



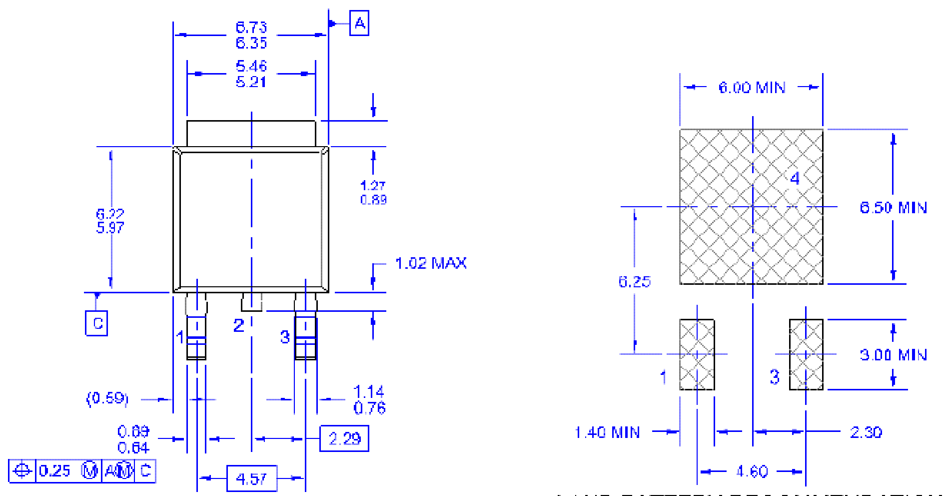
Peak Diode Recovery dv/dt Test Circuit & Waveforms



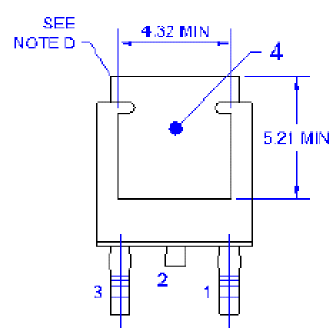


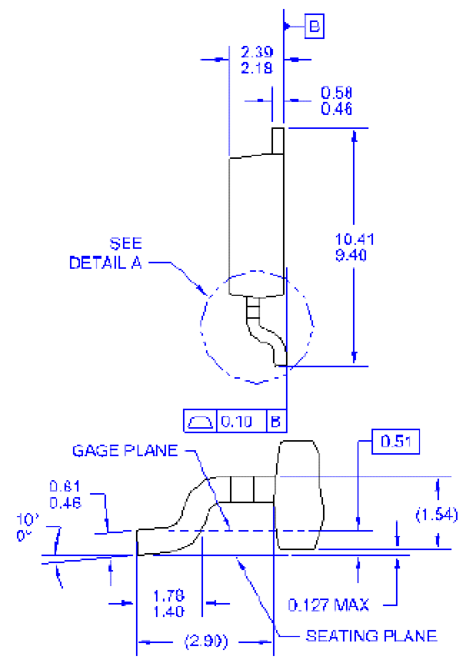
Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters

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